

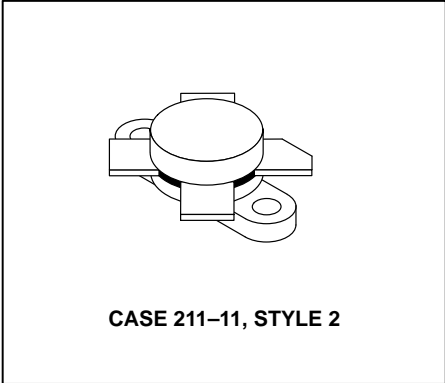
The RF MOSFET Line  
**RF Power**  
**Field-Effect Transistor**  
**N-Channel Enhancement-Mode**

**MRF255**

**55 W, 12.5 Vdc, 54 MHz**  
**N-CHANNEL**  
**BROADBAND**  
**RF POWER FET**

Designed for broadband commercial and industrial applications at frequencies to 54 MHz. The high gain, broadband performance and linear characterization of this device makes it ideal for large-signal, common source amplifier applications in 12.5 Volt mobile and base station equipment.

- Guaranteed Performance at 54 MHz, 12.5 Volts  
Output Power — 55 Watts PEP  
Power Gain — 13 dB Min  
Two-Tone IMD — -25 dBc Max  
Efficiency — 40% Min, Two-Tone Test
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Aluminum Nitride Package Electrical Insulator
- Circuit Board Photomaster Available by Ordering Document MRF255PHT/D from Motorola Literature Distribution.



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	36	Vdc
Drain-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	V <sub>DGR</sub>	36	Vdc
Gate-Source Voltage	V <sub>GS</sub>	±20	Vdc
Drain Current — Continuous	I <sub>D</sub>	22	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	175 1.0	Watts W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	1.0	°C/W

**Handling and Packaging** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain–Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 20$ mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 15$ Vdc, $V_{GS} = 0$ )	$I_{DSS}$	—	—	5.0	mAdc
Gate–Source Leakage Current ( $V_{GS} = 20$ Vdc, $V_{DS} = 0$ )	$I_{GSS}$	—	—	5.0	$\mu\text{Adc}$

**ON CHARACTERISTICS**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 25$ mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10$ Vdc, $I_D = 4.0$ Adc)	$V_{DS(on)}$	—	—	0.4	Vdc
Forward Transconductance ( $V_{DS} = 10$ Vdc, $I_D = 3.0$ Adc)	$g_{fs}$	4.2	—	—	S

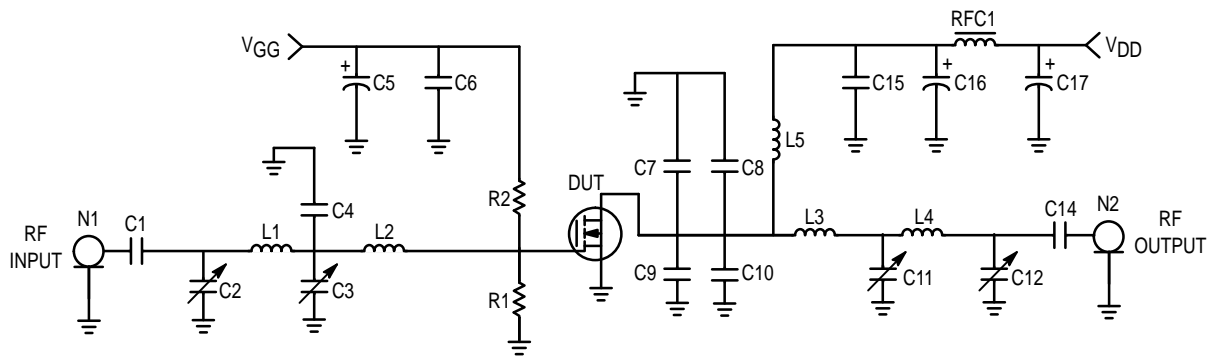
**DYNAMIC CHARACTERISTICS**

Input Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{iss}$	—	140	—	pF
Output Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{oss}$	—	285	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5$ Vdc, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{rss}$	—	38	44	pF

**FUNCTIONAL TESTS** (In Motorola Test Fixture.)

Common Source Amplifier Power Gain, $f_1 = 54$ , $f_2 = 54.001$ MHz ( $V_{DD} = 12.5$ Vdc, $P_{out} = 55$ W (PEP), $I_{DQ} = 400$ mA)	$G_{ps}$	13	16	—	dB
Intermodulation Distortion (1), $f_1 = 54.000$ MHz, $f_2 = 54.001$ MHz ( $V_{DD} = 12.5$ Vdc, $P_{out} = 55$ W (PEP), $I_{DQ} = 400$ mA)	$IMD_{(d3,d5)}$	—	–30	–25	dBc
Drain Efficiency, $f_1 = 54$ ; $f_2 = 54.001$ MHz ( $V_{DD} = 12.5$ Vdc, $P_{out} = 55$ W (PEP), $I_{DQ} = 400$ mA)	$\eta$	40	45	—	%
Drain Efficiency, $f = 54$ MHz ( $V_{DD} = 12.5$ Vdc, $P_{out} = 55$ W CW, $I_{DQ} = 400$ mA)	$\eta$	—	60	—	%
Output Mismatch Stress, $f_1 = 54$ ; $f_2 = 54.001$ MHz ( $V_{DD} = 12.5$ Vdc, $P_{out} = 55$ W (PEP), $I_{DQ} = 400$ mA, $V_{SWR} = 20:1$ , at all phase angles)	$\psi$	No Degradation in Output Power Before and After Test			

(1) To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

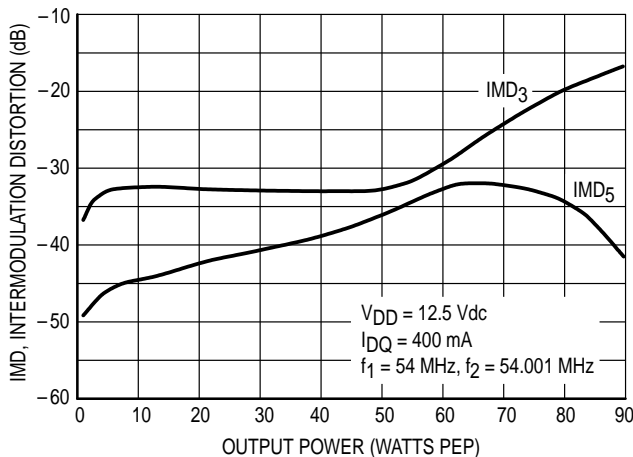


C1 — 470 pF, Chip Capacitor  
 C2, C3, C11, C12 — 20–200 pF, Trimmer, ARCO #464  
 C4 — 100 pF, Chip Capacitor  
 C5, C17 — 100  $\mu$ F, 15 V, Electrolytic  
 C6 — 0.001  $\mu$ F, Disc Ceramic  
 C7, C8, C9, C10 — 330 pF, Chip Capacitor  
 C14 — 1200 pF, ATC Chip Capacitor  
 C15 — 910 pF, 500 V, Dipped Mica  
 C16 — 47  $\mu$ F, 16 V, Electrolytic

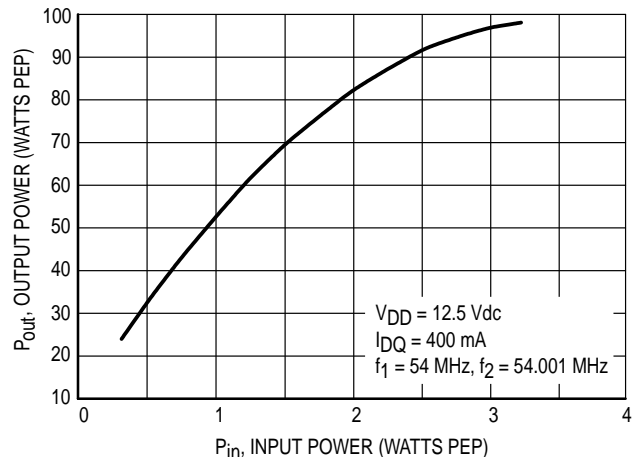
L1 — 8 Turns, #20 AWG, 0.126" ID  
 L2 — 5 Turns, #18 AWG, 0.142" ID  
 L3 — 3 Turns, #20 AWG, 0.102" ID  
 L4 — 7 Turns, #24 AWG, 0.070" ID  
 L5 — 6.5 Turns, #18 AWG, 0.230" ID, 0.5" Long  
 N1, N2 — Type N Flange Mount  
 RFC1 — Ferroxcube VK-200-19/4B  
 R1 — 39 k $\Omega$ , 1/4 W Carbon  
 R2 — 150  $\Omega$ , 1/4 W Carbon  
 Board — G-10 .060"

**Figure 1. 54 MHz Linear RF Test Circuit Electrical Schematic**

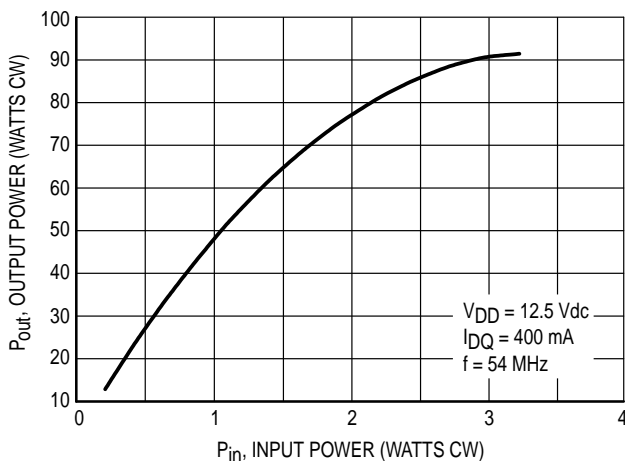
**TYPICAL CHARACTERISTICS**



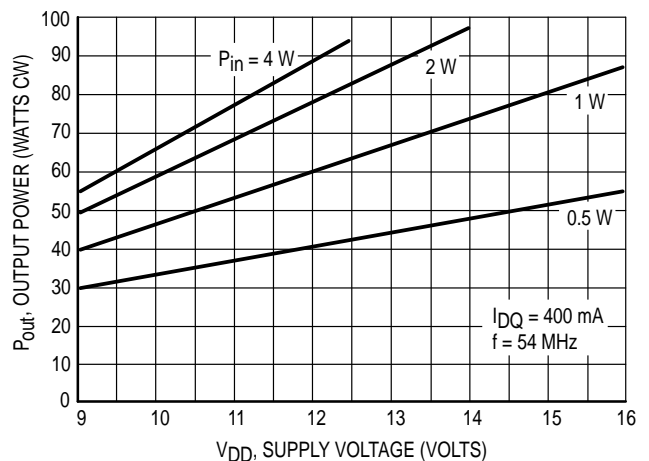
**Figure 2. IMD versus Output Power**



**Figure 3. Output Power versus Input Power**

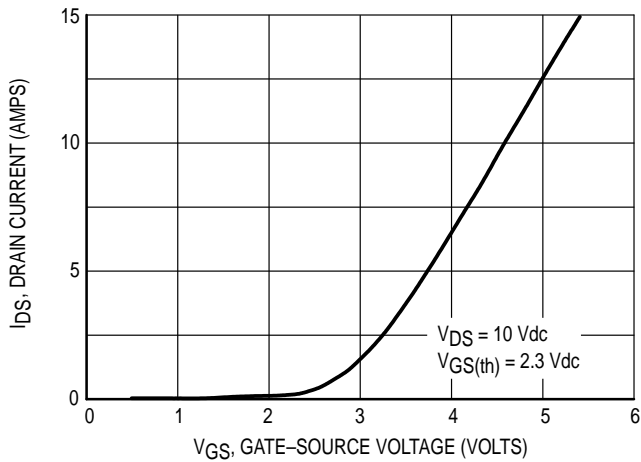


**Figure 4. Output Power versus Input Power**

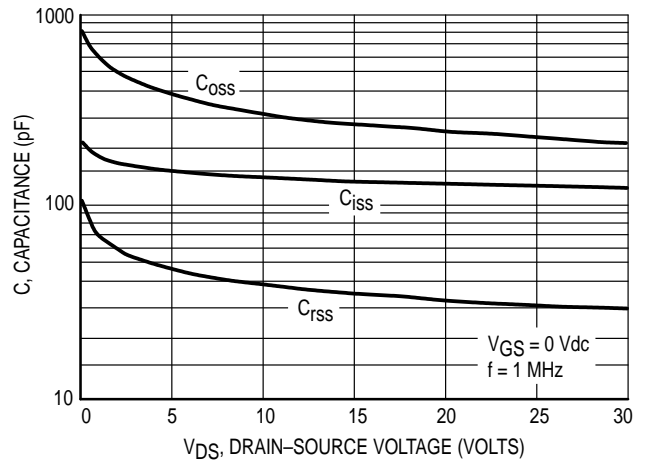


**Figure 5. Output Power versus Supply Voltage**

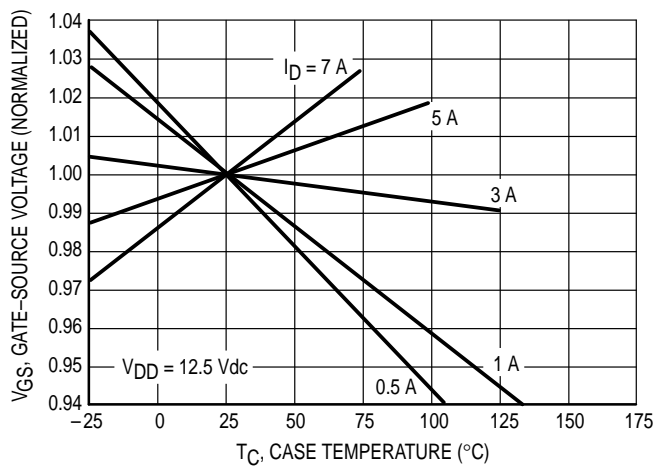
## TYPICAL CHARACTERISTICS



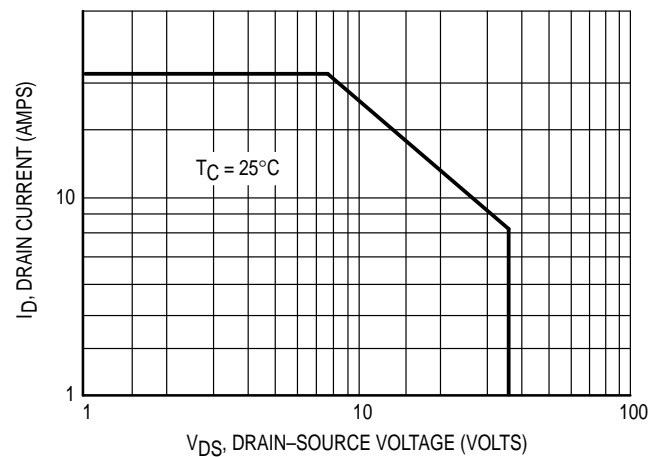
**Figure 6. Drain Current versus Gate Voltage**



**Figure 7. Capacitance versus Voltage**



**Figure 8. Gate-Source Voltage versus Case Temperature**



**Figure 9. DC Safe Operating Area**

**Table 1. Series Equivalent Input and Output Impedance**

$V_{DD} = 12.5 \text{ Vdc}$ ,  $I_{DQ} = 400 \text{ mA}$ ,  $P_{out} = 55 \text{ W PEP}$   
Optimized for Efficiency and IM Performance

f MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
54	$6.50 + j7.96$	$1.27 + j1.54$

$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device operates at a given power, voltage and frequency.

**Table 2. Common Source Scattering Parameters  
(V<sub>DS</sub> = 12.5 Vdc)**

**I<sub>D</sub> = 100 mA**

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ φ	S <sub>21</sub>	∠ φ	S <sub>12</sub>	∠ φ	S <sub>22</sub>	∠ φ
1	0.98	-32	39.6	161	0.013	71	0.32	-80
2	0.92	-60	34.6	145	0.023	56	0.50	-108
5	0.81	-110	21.3	118	0.035	29	0.75	-143
10	0.76	-140	11.9	102	0.039	14	0.83	-160
20	0.74	-158	6.08	90	0.040	4	0.86	-169
30	0.75	-163	4.03	82	0.039	-2	0.87	-173
40	0.75	-166	2.98	77	0.038	-5	0.87	-174
50	0.76	-167	2.35	72	0.037	-8	0.88	-175
60	0.78	-168	1.91	67	0.036	-10	0.89	-176
70	0.79	-168	1.60	63	0.034	-12	0.89	-176
80	0.80	-169	1.36	59	0.032	-13	0.90	-177
90	0.81	-169	1.18	56	0.031	-14	0.90	-177
100	0.82	-169	1.03	52	0.029	-15	0.91	-177
120	0.85	-170	0.81	46	0.025	-14	0.92	-178
140	0.87	-171	0.65	41	0.022	-11	0.93	-179
160	0.88	-172	0.54	37	0.019	-6	0.94	180
180	0.90	-173	0.45	33	0.017	2	0.95	179
200	0.91	-174	0.38	30	0.016	12	0.95	178
220	0.92	-175	0.33	27	0.016	23	0.96	177
240	0.93	-176	0.29	25	0.016	34	0.96	176
260	0.94	-177	0.25	23	0.018	44	0.97	175

**I<sub>D</sub> = 400 mA**

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ φ	S <sub>21</sub>	∠ φ	S <sub>12</sub>	∠ φ	S <sub>22</sub>	∠ φ
1	0.98	-46	56.6	155	0.008	66	0.45	-148
2	0.95	-80	46.1	137	0.013	48	0.64	-151
5	0.90	-129	25.1	113	0.017	25	0.84	-164
10	0.88	-153	13.4	100	0.019	14	0.89	-172
20	0.88	-167	6.82	91	0.019	10	0.91	-176
30	0.88	-171	4.55	87	0.019	9	0.91	-178
40	0.88	-173	3.41	83	0.019	10	0.91	-178
50	0.88	-175	2.72	80	0.019	11	0.91	-179
60	0.88	-176	2.25	78	0.019	12	0.91	-179
70	0.88	-176	1.92	75	0.019	14	0.92	-180
80	0.88	-177	1.67	72	0.019	16	0.92	180
90	0.89	-177	1.47	70	0.019	18	0.92	179
100	0.89	-178	1.31	68	0.019	20	0.92	179
120	0.89	-178	1.08	63	0.019	24	0.92	179
140	0.89	-179	0.90	59	0.019	29	0.93	178
160	0.90	-179	0.77	55	0.020	34	0.93	177
180	0.90	-180	0.67	52	0.021	38	0.93	177
200	0.91	180	0.59	48	0.022	43	0.94	176
220	0.91	179	0.53	45	0.023	47	0.94	175
240	0.91	179	0.47	42	0.025	50	0.95	175
260	0.92	178	0.43	40	0.026	53	0.95	174

**Table 2. Common Source Scattering Parameters (continued)**  
( $V_{DS} = 12.5$  Vdc)

$I_D = 1$  A

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ φ	S <sub>21</sub>	∠ φ	S <sub>12</sub>	∠ φ	S <sub>22</sub>	∠ φ
1	0.98	-54	65.5	152	0.006	63	0.60	-162
2	0.96	-91	50.9	133	0.009	44	0.75	-163
5	0.93	-137	26.2	110	0.011	23	0.88	-170
10	0.93	-158	13.7	99	0.012	15	0.91	-175
20	0.92	-169	6.96	92	0.012	15	0.92	-178
30	0.92	-173	4.65	89	0.012	18	0.93	-179
40	0.92	-175	3.49	86	0.013	21	0.93	-180
50	0.92	-176	2.79	84	0.013	25	0.93	180
60	0.92	-177	2.32	82	0.013	28	0.93	179
70	0.92	-178	1.99	80	0.014	31	0.93	179
80	0.92	-179	1.74	78	0.014	34	0.93	179
90	0.92	-179	1.54	76	0.015	37	0.93	178
100	0.92	-180	1.39	74	0.016	40	0.93	178
120	0.92	180	1.15	71	0.017	44	0.93	177
140	0.92	179	0.98	68	0.019	48	0.93	177
160	0.92	178	0.86	65	0.020	51	0.93	176
180	0.92	178	0.76	62	0.022	54	0.93	176
200	0.92	177	0.68	59	0.024	56	0.94	175
220	0.92	177	0.61	56	0.026	58	0.94	175
240	0.92	176	0.56	53	0.028	59	0.94	174
260	0.92	176	0.51	51	0.030	61	0.94	173

### DESIGN CONSIDERATIONS

The MRF255 is a common-source, RF power, N-channel enhancement mode Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

This device was designed primarily for HF 12.5 V mobile linear power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

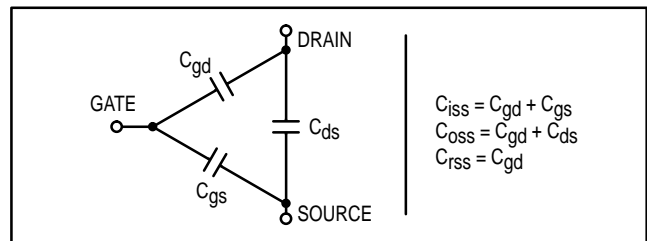
### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ).

These capacitances are characterized as input ( $C_{iSS}$ ), output ( $C_{oSS}$ ) and reverse transfer ( $C_{rSS}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iSS}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



### DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The drain-source voltage under these conditions is termed  $V_{DS(on)}$ . For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

## GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9$  ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change

on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

## DC BIAS

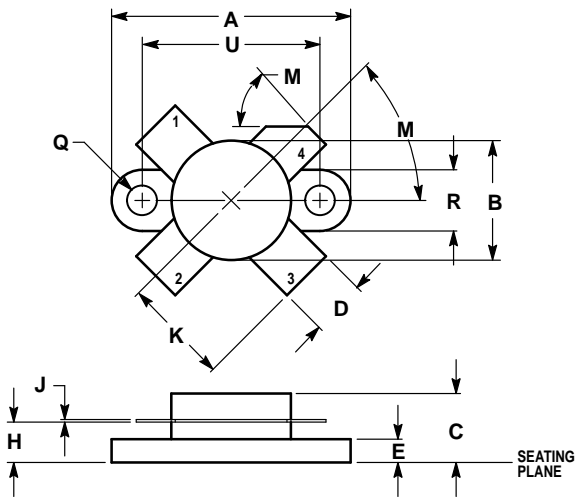
Since the MRF255 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. The MRF255 was characterized for linear and CW operation at  $I_{DQ} = 400$  mA, which is the suggested value of bias current for typical applications.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

## GAIN CONTROL

For CW applications, power output of the MRF255 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, AGC/ALC and modulation systems. The characteristic is very dependent on frequency and load line.

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45°NOM		45°NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

- STYLE 2:  
 PIN 1. SOURCE  
 2. GATE  
 3. SOURCE  
 4. DRAIN

**CASE 211-11  
ISSUE N**

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 P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**MFAX:** RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609  
**INTERNET:** http://Design-NET.com

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 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MRF255/D

